SC11805TP

freescale semiconductor

# FAX TRANSMITTAL SHEET

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24 Number of Pages (including this page)

Date: April 13, 2005

To: MS: APPEAL BRIEF-PATENTS

Location: United States Patent and Trademark Office

Fax No.: (703) 872-9306

From: Robert L. King (Registration No. 30,185)

Subject: S/N 10/074,732 – Leo Mathew et al.

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Date

Pat Thomas
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**MESSAGE:**

**Enclosed herewith is an Appeal brief for the above-referenced patent application.**

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED IN THE FAX

| | | |
|---|---|---|
| 1. | x | 1 page Fax cover sheet |
| 2. | x | 1 page Fee Transmittal (in duplicate) |
| 3. | x | 21 page Notice of Appeal |

Fees charged to Deposit Account 503079, Freescale Semiconductor, Inc. $500

# FEE TRANSMITTAL

Patent fees are subject to annual revision

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500

| Complete if Known | |
|---|---|
| Application Number | 10/074,732 |
| Filing Date | February 13, 2002 |
| First Named Inventor | Leo Mathew et al. |
| Examiner Name | Paul E. Brock II |
| Group Art Unit | 2815 |
| Attorney Docket No. | SC11805TP |

## METHOD OF PAYMENT (check all that apply)

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## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | | Fee Paid |
|---|---|---|---|---|---|
| 1011 | 300 | 2011 | 150 | Utility filing fee | 300 |
| 1111 | 500 | 2111 | 250 | Utility search fee | 500 |
| 1311 | 200 | 2311 | 100 | Utility Exam fee | 200 |
| 1002 | 300 | 2002 | 175 | Design filing fee | |
| 1003 | 550 | 2003 | 275 | Plant filing fee | |
| 1004 | 790 | 2004 | 395 | Reissue filing fee | |
| 1005 | 200 | 2005 | 100 | Provisional filing fee | |

SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES

| | | Previously Paid** | | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|---|---|---|
| Total Claims | | - 20 | = | | X | 50 | = | |
| Independent Claims | | - 3 | = | | X | 200 | = | |
| Multiple Dependent | | | | | | 360 | = | |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 50 | 2202 | 25 | Claims in excess of 20 |
| 1201 | 200 | 2201 | 100 | Independent claims in excess of 3 |
| 1203 | 360 | 2203 | 180 | Multiple dependent claim, if not paid |
| 1204 | 88 | 2204 | 44 | * Reissue Independent claims over original patent |
| 1205 | 200 | 2205 | 100 | *Reissue claim s in excess of 20 and over original patent |

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above.

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge – late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge – late Provisional filing | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2520 | 1812 | 2520 | For filing a request for ex parte Reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1840* | 1805 | 1840* | Requesting publication of SIR after Examiner action | |
| 1251 | 120 | 2251 | 60 | Extension for reply within first month | |
| 1252 | 450 | 2252 | 225 | Extension for reply within second month | |
| 1253 | 1020 | 2253 | 510 | Extension for reply within third month | |
| 1254 | 1590 | 2254 | 795 | Extension for reply within fourth month | |
| 1255 | 2160 | 2255 | 1080 | Extension for reply within fifth month | |
| 1401 | 500 | 2401 | 250 | Notice of Appeal | |
| 1402 | 500 | 2402 | 250 | Filing a brief in support of an appeal | 500 |
| 1403 | 1000 | 2403 | 500 | Request for oral hearing | |
| 1451 | 1510 | 1451 | 1510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive – unavoidable | |
| 1453 | 1370 | 2453 | 685 | Petition to revive – unintentional | |
| 1501 | 1400 | 2501 | 700 | Utility issue fee (or reissue) | |
| 1502 | 800 | 2502 | 400 | Design issue fee | |
| 1503 | 1100 | 2503 | 550 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 130 | 1807 | 130 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of IDS | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 790 | 2809 | 395 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 1810 | 790 | 2810 | 395 | For each additional invention to be examined (37 CFR § 1.129(b)) | |
| 1801 | 790 | 2801 | 395 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify)

SUBTOTAL (3) ($) 500

* Reduced by Basic Filing Fee Paid

## SUBMITTED BY

Complete (if applicable)

| Name (Print/Type) | Robert L. King | Registration No. | 30,185 | Telephone | (512) 996-6839 |
|---|---|---|---|---|---|
| Signature | Robert L. King | Date | April 13, 2005 | | |

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| Attorney Docket No. | SC11805TP |

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SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES

| | | Previously Paid** | | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|---|---|---|
| Total Claims | | - 20 | = | | X | 50 | = | |
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| 1201 | 200 | 2201 | 100 | Independent claims in excess of 3 |
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## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

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| 1801 | 790 | 2801 | 395 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify)

SUBTOTAL (3) ($) 500

* Reduced by Basic Filing Fee Paid

## SUBMITTED BY

Complete (if applicable)

| Name (Print/Type) | Robert L. King | Registration No. | 30,185 | Telephone | (512) 996-6839 |
|---|---|---|---|---|---|
| Signature | Robert L. King | Date | April 13, 2005 | | |

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DOCKET NO. SC11805TP

UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| APPLICANT | Leo Mathew et al. | GROUP ART UNIT: | 2815 |
| APPLN. NO.: | 10/074,732 | EXAMINER: | Paul E Brock II |
| FILED: | February 13, 2002 | CONFIRMATION No.: | 6470 |
| TITLE: | METHOD OF FORMING A VERTICAL DOUBLE GATE SEMICONDUCTOR DEVICE | | |

Certificate of Transmission under 37 C.F.R 1.8

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on 4-13-05

(Pat Thomas)

Signature PAT THOMAS

Printed Name of Person Signing Certificate

# APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

## REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin, Texas.

## RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

## STATUS OF CLAIMS

Claims 1, 2, 4, 5, 7-12, 14-21, 24, 25 and 34 are pending and involved in this appeal. Claims 35 and 36 are withdrawn from consideration. Claim 1 was previously presented. Claim 2 is original. Claim 3 has been canceled. Claims 4 and 5 were previously presented. Claim 6 has been canceled. Claims 7-12 were previously presented. Claim 13 has been canceled. Claims 14-17 were previously presented. Claims 18-21 are original. Claim 22 has been canceled. Claims 23-25 are original. Claims 26-33 have been canceled. Claim 34 was previously presented.

Claims 1-2, 4, 5, 7-12, 14, 16-25 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al., U.S. Patent No. 6,472,258 (Adkisson et al.) in view of Fried et al. (U.S. Pub. 2003/0113970 (Fried et al.)). Claim 15 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. and Fried et al. as applied to claims 1 and 11, and further in view of Forbes et al., U.S. Patent No. 6,414,356 (Forbes et al.).

The rejection of claims 1, 2, 4, 5, 7-12, 14-21, 24, 25 and 34 is being appealed.

## STATUS OF AMENDMENTS

A most recent amendment filed on June 9, 2004 was entered. A final rejection was mailed on December 10, 2004. No further amendments were filed after the final rejection.

## SUMMARY OF THE INVENTION

Independent claim 1 recites a method of forming a vertical double gate semiconductor device. As illustrated in FIG. 1 and described on page 4, lines 14-21 of the specification, a substrate is provided with an overlying first insulating layer and an overlying first semiconductor layer. As illustrated in FIG. 2 and described on page 4, line 21 to page 5, line 7, portions of the first semiconductor layer are removed to form a semiconductor structure having a first sidewall and an opposite second sidewall. A second insulating layer is formed adjacent the sidewalls as illustrated in FIG. 3 as described on page 5, lines 8-17. A second semiconductor layer is provided over and adjacent the semiconductor structure as illustrated in FIG. 3 and described on page 5, lines 8-17. A first directional implant of a first conductivity type is performed from a first direction as illustrated in FIG. 4 and described on page 5, line 18 to page 6, line 6. A second directional implant of a second and opposite conductivity type is preformed from a second direction as illustrated in FIG. 6 and described on page 6, line 18 to page 7, line 12. A conductive layer is formed over the semiconductor structure and the second insulating layer as illustrated in FIG. 10 and described on page 9, lines 1-12. A portion of the conductive layer and the second semiconductor layer is removed to physically separate a first gate region and a second gate region as illustrated in FIGs. 11 and 12 and described on page 9, line 13 to page 10, line 17. The first gate region is adjacent the first sidewall and has a first conductivity type and the second gate region is adjacent the second sidewall and has an opposite second conductivity type. Because the two gate regions are physically separate, the semiconductor structure prevents migration of doping species between the two gate regions.

Independent claim 17 recites a method of forming a vertical double gate semiconductor device. As illustrated in FIG. 1 and described on page 4, lines 14-21 of the specification, a substrate is provided with an overlying first insulating layer and an overlying first semiconductor layer. As illustrated in FIG. 2 and described on page 4, line 21 to page 5, line 7, portions of the

first semiconductor layer are etched to form a semiconductor structure having a first sidewall and an opposite second sidewall. A source region and a drain region are formed overlying the substrate in a second direction as illustrated in FIG. 16 and described on page 11, line 21 to page 12, line 9. A second insulating layer (element 26) is formed adjacent the sidewalls as illustrated in FIG. 3 as described on page 5, lines 8-17. A second semiconductor layer (element 28) is provided over and adjacent the semiconductor structure as illustrated in FIG. 3 and described on page 5, lines 8-17. The second semiconductor layer has three recited portions: (1) adjacent the first sidewall; (2) over the semiconductor structure; and (3) adjacent the second sidewall. The first portion is doped with a first species (FIG. 4) and the third portion is doped with a second species opposite the first portion (FIG. 6). The second portion is subsequently removed (FIG. 8) to physically separate the first portion and the third portion. The semiconductor structure is recited having the first sidewall and the second sidewall. The specification in FIG. 8 illustrates the sidewalls to comprise, in one form, the sides of nitride layer 22, pad oxide 20 and insulating gate dielectric 26 as described at page 4, line 22 to page 5, line 11, all of which are insulating. The specification teaches at page 5, line 12 to line 17 that the semiconductor layer that corresponds to the recited first portion and third portion has a material composition that is conductive or semiconductive and therefore differs at all adjoining surfaces from the material composition of the recited semiconductor structure.

Independent claim 34 recites a method of forming a vertical double gate semiconductor device. As illustrated in FIG. 1 and described on page 4, lines 14-21 of the specification, a substrate is provided with an overlying first insulating layer and an overlying first semiconductor layer. As illustrated in FIG. 2 and described on page 4, line 21 to page 5, line 7, a semiconductor structure (element 24) overlies the substrate and has opposing first and second sidewalls. An insulating layer (element 26) is formed adjacent the sidewalls as illustrated in FIG. 3 as described on page 5, lines 8-17. A semiconductor layer (element 28) is provided over and around the semiconductor structure as illustrated in FIG. 3 and described on page 5, lines 8-17. The

semiconductor layer has three recited portions: (1) adjacent the first sidewall and having a first non-horizontal surface; (2) adjacent the second sidewall and having a second non-horizontal surface; and (3) over the semiconductor structure. The device is doped with two angled implants of opposite conductivity (FIGs. 4 and 6) resulting in the first and second portions having opposite conductivity and the third portion having a mixed species doping. The third portion is subsequently removed (FIG. 8) to physically separate the first portion and the second portion via the semiconductor structure to substantially eliminate migration of doping species between the first portion and the second portion.

## GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-2, 4, 5, 7-12, 14, 16-25 and 34 made obvious in view of the combination of Adkisson et al. and Fried et al.?

2) Is claim 15 made obvious in view of the combination of Adkisson et al., Fried et al. and Forbes?

## ARGUMENTS

### Arguments for Ground 1

Independent Claim 1

Independent claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al. in view of Fried et al. The stated basis for the rejection has remained identical for several Office Actions. Therefore Applicants will direct the Board's attention to pages 3-5 of the final Office Action. Figures 1, 2 and 3 of Adkisson et al. are relied upon as making claim 1 obvious. Adkisson et al. disclose in FIG. 1 a process in which a monocrystalline layer 14 is deposited over buried oxide 12. A layer of silicon nitride 16 is deposited. At Col. 3, lines 20-29

is described the opening of the silicon nitride and etching of the layer 14 to the buried oxide to result in the structure of FIG. 1. At Col. 3, lines 30-49 is described processing to result in the structure of FIG. 2. The layer 14 is further etched to underlie only a portion of the overlying silicon nitride 16 and gate material 20 is deposited, polished and recessed below the nitride surface. Both polishing and etching are required according to Col. 3, lines 44-46. Alternatives are illustrated in FIG. 3. In these forms adjacent silicon nitride is not present and sidewall spacers or sidewall liners are placed on outer exposed surfaces of the two polysilicon gates.

It should be noted in the Adkisson et al. patent that there is no teaching of "providing a second semiconductor layer over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure and having a non-horizontal surface adjoining the semiconductor structure" as recited in claim 1. There is no teaching by Adkisson et al. of "providing a first directional implant of a first conductivity type". There is no teaching by Adkisson et al. of "providing a second directional implant of a second conductivity type". In addition to not teaching directional implants, Adkisson et al. do not teach that the double gates are oppositely doped in conductivity. At Col. 3, lines 6-11, Adkisson et al. only state that doping levels are relatively low and provide a range of preferred levels. Therefore, there is no teaching or suggestion of using a semiconductor structure for "preventing migration of doping species between the first gate region and the second gate region" as recited in claim 1.

Fried et al. disclose an asymmetric doped FINFET having a continuously conductive gate above and adjacent the fin structure of the FINFET. For example, in paragraph 31 there is described asymmetric implants in gate portions 24 and 26 that are connected together by a double implant region 28 that permits migration of doping species between gate portions 24 and 26 to occur. Fried et al. do not teach or suggest that the presence of the double implant region 28 in contact with the single implant regions is detrimental to the operation of the transistor. Cross

migration of dopants leads to part of the gate structure functioning in a depletion mode or a very high transistor threshold voltage mode.

Fried et al. do not teach or suggest "removing a portion of the conductive layer and the second semiconductor layer to physically separate a first gate region and a second gate region" as recited in claim 1. Fried et al. do not teach or suggest "the semiconductor structure preventing migration of doping species between the first gate region and the second gate region".

If Adkisson et al. and Fried et al. are combined, there is no teaching or suggestion by the combination to prevent the cross-migration of a FINFET having asymmetric gate doping. To so state is to use hindsight reconstruction of Applicants' teaching and apply them to a combination of references and then state that it could be possible. The burden of showing an actual teaching of the recited subject matter of claim 1 has not been met.

During the application's prosecution, Applicants advocated to the Examiner that applying angle implanting to the Adkisson et al. structure of figure 2 or figure 3 would not result in gate regions having a single doping type. A basis for Applicants' position is found in the next to last sentence of paragraph 31 of Fried et al. there is stated "Due to the shadowing of the structure, the gate sides (i.e., vertical portions of polysilicon-containing layer 18) remain doped (either N+ or P+) with the species implanted from that side, while the horizontal portions of polysilicon-containing layer 18 are counterdoped, i.e., double implanted". The gate polysilicon in figure 2 and figure 3 of Adkisson et al. has only exposed horizontal surfaces. Angle implanting the Adkisson et al. device will create counterdoped gate regions consistent with the patent of Fried et al. and result in modified threshold voltage of the transistor.

During the application's prosecution, Applicants also advocated that the gate structure of the Fried et al. device was a single gate structure having portions that are differently doped. The final rejection basis refutes this statement by stating that the Fried et al. device is only directed to a double gate device of oppositely doped portions 24 and 26 separated by counter doped portion 28 that is "not conductive enough (if at all) to interfere with the first and second gate

interaction". This conclusion is not supported by Fried et al. and is not technically supportable. Fried et al. describe in paragraph 36 that the counterdoped areas that are double implanted and are designated by reference number 28, are conductive. In paragraph 36 of the Fried et al. patent, there is described a conductive metallic silicide layer 36 that "eliminates the pn junction in the gate". The pn junction in the gate exists because the counterdoped regions are not insulating or nonconductive as assumed in the rejection basis. Fried et al. also teach in paragraph 36 that the metallic silicide layer 36 makes contact between layer 34 and the double implanted regions 28 as further evidence that the double implanted regions are conductive. Fried et al. clearly teach a single gate structure having portions that are differently doped. Therefore, Applicants continue to point out that the teachings of Fried et al. and Adkisson et al. are very different with respect to gate structure as Fried et al. are teaching an electrically continuous gate and Adkisson et al. are teaching a device with electrically separate gates.

In conclusion, the combination of Adkisson et al. and Fried et al. does not make claim 1 obvious. Applicants have invented an improved method for forming a double gate semiconductor device that has enhanced performance from known semiconductor devices.

Dependent claims 2, 4, 5, 7-12 and 14-16

Dependent claims 2, 4, 5, 7-12 and 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al. in view of Fried et al.. Each of these claims is patentable over the combination of these references at least as a result of being dependent from claim 1 for the reasons provided above. It should be noted that processing details associated with forming a completed transistor are not provided by either Adkisson et al. or Fried et al. outside of the formation of the gate structure.

Independent claim 17

Independent claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al. in view of Fried et al. The stated basis for the rejection has remained identical for several Office Actions. Therefore Applicants will direct the Board's attention to pages 8-9 of the final Office Action. Figures 1, 2 and 3 of Adkisson et al. are relied upon as making claim 17 obvious. Adkisson et al. disclose in FIG. 1 a process in which a monocrystalline layer 14 is deposited over buried oxide 12. A layer of silicon nitride 16 is deposited. At Col. 3, lines 20-29 is described the opening of the silicon nitride and etching of the layer 14 to the buried oxide to result in the structure of FIG. 1. At Col. 3, lines 30-49 Adkisson et al. describe processing to create the structure of FIG. 2. The layer 14 is further etched to underlie only a portion of the overlying silicon nitride 16 and gate material 20 is deposited, polished and recessed below the nitride surface. Both polishing and etching are required according to Col. 3, lines 44-46. Alternatives are illustrated in FIG. 3. In these forms adjacent silicon nitride is not present and sidewall spacers or sidewall liners are placed on outer exposed surfaces of the two polysilicon gates.

It should be noted in the Adkisson et al. there is no teaching of "forming a second semiconductor layer over and adjacent the semiconductor structure and the second insulating layer, wherein the second semiconductor layer comprises: a first semiconductor portion which is adjacent the first sidewall and having a first non-horizontal surface; a second semiconductor portion which is over the semiconductor structure; and a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal surface" as recited in claim 17. There is no teaching by Adkisson et al. of "doping the first semiconductor portion with a first series and doping the third semiconductor portion with a second species opposite the first species". In addition Adkisson et al. do not teach that the double gates are oppositely doped in conductivity. At Col. 3, lines 6-11, Adkisson et al. only state that doping levels are relatively

low and provide a range of preferred levels. Therefore, there is no teaching or suggestion of using a semiconductor structure for "preventing migration of doping species between the first gate region and the second gate region" as recited in claim 17.

Fried et al. disclose an asymmetric doped FINFET having a continuously conductive gate above and adjacent the fin structure of the FINFET. For example, in paragraph 31 there is described asymmetric implants in gate portions 24 and 26 that are connected together by a double implant region 28 that permits migration of doping species between gate portions 24 and 26 to occur. Fried et al. do not teach or suggest that the presence of the double implant region 28 in contact with the single implant regions is detrimental to the operation of the transistor. Cross migration of dopants leads to part of the gate structure functioning in a depletion mode or a very high transistor threshold voltage mode.

Fried et al. do not teach or suggest "removing the second semiconductor portion to physically separate the first semiconductor portion and the third semiconductor portion via the semiconductor structure" as recited in claim 17. Fried et al. do not teach or suggest "to substantially eliminate migration of doping species between the first semiconductor portion and the third semiconductor portion".

If Adkisson et al. and Fried et al. are combined, there is no teaching or suggestion by the combination to prevent the cross-migration of a FINFET having asymmetric gate doping. To so state is to use hindsight reconstruction of Applicants' teaching and apply them to a combination of references and then state that it could be possible. The burden of showing an actual teaching of the recited subject matter of claim 1 has not been met.

In the previous responses, Applicants advocated to the Examiner that applying angle implanting to the Adkisson et al. structure of figure 2 or figure 3 would not result in single doped gate regions. A basis for Applicants' position is found in the next to last sentence of paragraph 31 of Fried et al. there is stated "Due to the shadowing of the structure, the gate sides (i.e., vertical portions of polysilicon-containing layer 18) remain doped (either N+ or P+) with the

species implanted from that side, while the horizontal portions of polysilicon-containing layer 18 are counterdoped, i.e., double implanted". The gate polysilicon in figure 2 and figure 3 of Adkisson et al. has only exposed horizontal surfaces. Angle implanting the Adkisson et al. device will create counterdoped gate regions resulting in modified threshold voltage of the transistor.

In conclusion, the combination of Adkisson et al. and Fried et al. does not make claim 17 obvious. Applicants have invented an improved method for forming a double gate semiconductor device that has enhanced performance from known semiconductor devices.

Dependent claims 18-21 and 23-25

Dependent claims 18-21 and 23-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al. in view of Fried et al.. Each of these claims is patentable over the combination of these references at least as a result of being dependent from claim 17 for the reasons provided above.

Independent claim 34

Independent claim 34 stands rejected under 35 U.S.C. § 103(a) as being unpatentable on the basis that "is similar to the rejection of claims 1 and 17 above using Adkisson in view of Fried". Therefore, the subject matter of Adkisson et al. and Fried et al. will not be repeated. Claim 34 is allowable over this combination of references as the combination does not teach or suggest both "doping the device with two angled implants of opposite conductivity type, the first semiconductor portion having a resulting first conductivity, the second semiconductor portion having a resulting second conductivity and the third semiconductor portion having mixed species doping" and "removing the third semiconductor portion to physically separate the first semiconductor portion and the second semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and

the second semiconductor portion". The comments provided above directly address how Adkisson et al. and Fried et al. do not teach or anticipate these claim recitals.

## Arguments for Ground 2

### Dependent claim 15

Claims 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Adkisson et al. and Fried as applied to claims 1 and 11 above, and further in view of Forbes et al. (U.S. Patent 6,414,356). In the rejection, Forbes et al. is cited for teaching annealing a first gate region and a second electrode region before forming a metal. The dual-gated transistor structures described by Forbes et al. is otherwise significantly dissimilar to the structure claimed in claim 15 by having physically separate and mirrored gates overlying the same channel region. The base limitations of claim 15 are readily distinguishable from this combination of three references for at least the reasons stated above in connection with claims 11 and 1. In semiconductor processing, heat processing and metal deposition are common steps. However, this combination of references does not teach the manufacturing method recited therein with the timing of an anneal prior to depositing metal.

Further evidence of the standard of obviousness is this art area is noted by the Examiner in the final rejection. Claims 35 and 36 associated with this application in which doping of sidewall spacers after the sidewall spacers are physically separated were deemed by the Examiner to be patentably separate and distinct inventions from a method where doping of sidewall spacers occurs before the sidewall spacers are physically separated. Applicants were required to withdraw claims 35 and 36 from this Board's consideration on the basis that the order of those two steps is patentably distinct. Similarly, the use and order of annealing and metal deposition in a double gate process not taught by a combination of three references is not made

obvious by the fact that prior art transistor gate formation processes utilize thermal processing and metal deposition.

## CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,
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# Claims Appendix

1. (Previously Presented) A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

providing a first insulating layer over the semiconductor substrate;

providing a first semiconductor layer over the first insulating layer;

removing portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall;

forming a second insulating layer adjacent the first sidewall and the second sidewall;

providing a second semiconductor layer over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure and having a non-horizontal surface adjoining the semiconductor structure;

performing a first directional implant of a first conductivity type of the second semiconductor layer from a first predetermined direction;

performing a second directional implant of a second conductivity type opposite the first conductivity type of the second semiconductor layer from a second predetermined direction that differs from the first predetermined direction;

forming a conductive layer over the semiconductor structure and the second insulating layer; and

removing a portion of the conductive layer and the second semiconductor layer to physically separate a first gate region and a second gate region, wherein:

the first gate region is adjacent the first sidewall of the semiconductor structure and has the first conductivity type; and

the second gate region is adjacent the second sidewall of the semiconductor structure and has the second conductivity type, the

semiconductor structure preventing migration of doping species between the first gate region and the second gate region.

2. (Original) The method of claim 1 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

Claim 3 (Canceled)

4. (Previously Presented) The method of claim 1 wherein removing the portion of the conductive layer and the second semiconductor layer comprises planarizing the second semiconductor layer and the conductive layer.

5. (Previously Presented) The method of claim 1 further comprising forming a first current electrode region and a second current electrode region in the semiconductor substrate to implement the vertical double gate semiconductor device as a transistor.

Claim 6 (Canceled)

7. (Previously Presented) The method of claim 1, wherein each of the first directional implant and the second directional implant is performed by ion implantation at symmetric opposing angles relative to a top surface of the semiconductor substrate.

8. (Previously Presented) The method of claim 1, further comprising annealing the first gate region and the second gate region after the first directional implant and the second directional implant.

9. (Previously Presented) The method of claim 1, wherein removing a portion of the conductive layer is performed after performing the second directional implant of the second conductivity type.

10. (Previously Presented) The method of claim 1 further comprising electrically coupling the first gate region and the second gate region.

11. (Previously Presented) The method of claim 1, further comprising forming a metal layer as the conductive layer.

12. (Previously Presented) The method of claim 1, wherein forming the conductive layer comprises:

forming a silicon layer over the first gate region, the second gate region, and the semiconductor structure;

forming a first metal layer over the silicon layer; and

heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide.

Claim 13 (Canceled)

14. (Previously Presented) The method of claim 13, wherein removing a portion of the conductive layer comprises planarizing the conductive layer.

15. (Previously Presented) The method of claim 11, further comprising annealing the first gate region and the second gate region before forming the metal layer.

16. (Previously Presented) The method of claim 11, wherein the metal layer further comprises a stack of metal layers.

17. (Previously Presented) A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a first insulating layer over the semiconductor substrate;

forming a first semiconductor layer on the first insulating layer;

etching portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming a source region and a drain region overlying the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction;

forming a second insulating layer on the first sidewall and the second sidewall;

forming a second semiconductor layer over and adjacent the semiconductor structure and the second insulating layer, wherein the second semiconductor layer comprises:

a first semiconductor portion which is adjacent the first sidewall and having a first non-horizontal surface;

a second semiconductor portion which is over the semiconductor structure; and

a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal surface;

doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species opposite the first species; and

subsequently removing the second semiconductor portion to physically separate the first semiconductor portion and the third semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the third semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the third semiconductor portion at all adjoining surfaces.

18. (Original) The method of claim 17, wherein the second insulating layer is deposited conformally.

19. (Original) The method of claim 17 further comprising annealing the second semiconductor layer.

20. (Original) The method of claim 19 wherein annealing is performed after removing the second semiconductor portion.

21. (Original) The method of claim 17 wherein removing the second portion is performed by a method selected from the group of anisotropic etching, planarization and etch back.

Claim 22 (Canceled)

23. (Original) The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion is performed by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

24. (Original) The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer over the semiconductor substrate.

25. (Original) The method of claim 17, wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises:

forming a third insulating layer over the first semiconductor layer;

forming a nitride layer over the third insulating layer;

patterning the nitride layer and the third insulating layer; and

etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

Claims 26-33 (Canceled)

34. (Previously Presented) A method for forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a semiconductor structure overlying the substrate and having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming an insulating layer on the first sidewall and the second sidewall;

forming a semiconductor layer over and around the semiconductor structure and the insulating layer, wherein the semiconductor layer comprises:

a first semiconductor portion which is adjacent the first sidewall and having a first surface that is non-horizontal;

a second semiconductor portion which is adjacent the second sidewall and having a second surface that is non-horizontal; and

a third semiconductor portion overlying the semiconductor structure;

doping the device with two angled implants of opposite conductivity type, the first semiconductor portion having a resulting first conductivity, the second semiconductor portion having a resulting second conductivity and the third semiconductor portion having mixed species doping; and

removing the third semiconductor portion to physically separate the first semiconductor portion and the second semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the second semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the second semiconductor portion at all adjoining surfaces.

35. (Withdrawn) A method for forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a semiconductor structure overlying the substrate and having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming an insulating layer on the first sidewall and the second sidewall;

forming a semiconductor layer over and around the semiconductor structure and the insulating layer, wherein the semiconductor layer;

removing regions of the semiconductor layer having a substantially horizontal exposed surface, the regions of the semiconductor layer overlying the semiconductor structure and the semiconductor substrate to form a first sidewall spacer and a second sidewall spacer that are physically separated; and

doping the first and second physically separated sidewall spacers with two angled implants of opposite conductivity type, the first sidewall spacer having a resulting first conductivity and the second sidewall spacer having a resulting second conductivity.

36. (Withdrawn) The method of claim 35 further comprising:

electrically coupling the first and second physically separated sidewall spacers together.

# Evidence Appendix Under 37 CFR 41.37(c)(1)(ix)

There is no evidence that has been entered into the record by the Examiner that is relied upon in this appeal.